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## By P., H. Gundlach, R. Van Rissen, Et Al Varma

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6th IEEE International Workshop on Testing Embedded Core-Based System-Chips. Hyatt Regency, Monterey, California, USA May 1-2, 2002

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Bibliographic content of IEEE VLSI Test Symposium 2001. Marina Del Rey, CA, USA. Trier 1. Trier 2; Codes with Application to System-on-a-Chip Test Data

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(DFT), VLSI chip yield, VLSI Test Principles and Architectures, Elsevier, 2006. Asian Test Symposium (ATS)

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